GATE DRIVING CIRCUIT AND DISPLAY APPARATUS INCLUDING THE SAME

[0001] This application claims priority to Korean Patent Application No. 10-2016-0145322, filed on Nov. 2, 2016, and all the benefits accruing therefrom under 35 U.S.C. § 119, the content of which in its entirety is herein incorporated by reference.

BACKGROUND

(a) Field

[0002] The disclosure relates to a gate driving circuit and a display device including the gate driving circuit, and more particularly, to a gate driving circuit with improved display quality and a display device including the gate driving circuit.

(b) Description of the Related Art

[0003] A display device typically includes a plurality of gate lines, a plurality of data lines, and a plurality of pixels that are connected to the plurality of gate lines and the plurality of data lines. The display device may further include a gate driving circuit that provides gate signals to the plurality of gate lines and a data driving circuit that provides data signals to the plurality of data lines.

[0004] The gate driving circuit may include a shift resistor that includes a plurality of driving stage circuits (hereinafter will be referred to as driving stages). The plurality of driving stages output gate signals that respectively correspond to the plurality of gate lines. Each of the plurality of driving stages includes a plurality of transistors that are organically connected to each other.

[0005] A driving characteristic of some transistors among the plurality of transistors may be changed such that reliability of the gate driving circuit is deteriorated, and a current is leaked through the transistor such that an image may not be normally displayed in the display device.

SUMMARY

[0006] In such a display device, driving characteristics of some transistors among the plurality of transistors therein may be changed such that reliability of the gate driving circuit is deteriorated, and a current may be leaked through some transistors such that an image may not be normally displayed.

[0007] Exemplary embodiments relate to a gate driving circuit that compensates a change of a threshold voltage of some of transistors therein, and a display device including the gate driving circuit.

[0008] Exemplary embodiments relate to a gate driving circuit with improved reliability and a display device including the gate driving circuit.

[0009] In an exemplary embodiment, a gate driving circuit includes a plurality of stages which outputs gate signals to corresponding gate lines, respectively. In such an embodiment, a stage of the plurality of stages includes: a first control transistor diode-connected between a first input end of the stage and a first node, where the first control transistor is biased by a first input signal of the first input end of the stage, and back-biased by a second input signal of a second input end of the stage; a second control transistor including a control end connected to a third input end of the stage and which receives a third input signal, a first end connected to the first node, and a second end connected to a first voltage, where the second control transistor is back-biased by a fourth input signal of a fourth input end of the stage; a first output transistor including a control end connected to the first node, a first end connected to a clock input end of the stage, and a second end connected to a first output end of the stage; and a capacitor connected between the control end of the first output transistor and the second end of the first output transistor. In such an embodiment, the second input signal and the fourth input signal have enable levels during different periods from each other.

[0010] In an exemplary embodiment, the stage of the plurality of stages may further include: a second output transistor including a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a second output end of the stage to output a carry signal; and a third output transistor including a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a third output end of the stage to output a compensation signal, where the second output transistor may be back-biased by the compensation signal.

[0011] In an exemplary embodiment, the second input signal may be a compensation signal output from a previous stage of the stage, among the plurality of stages.

[0012] In an exemplary embodiment, the fourth input signal may be a to compensation signal output from a next stage of the stage, among the plurality of stages.

[0013] In an exemplary embodiment, the stage of the plurality of stages may further include: an inverter which outputs a signal synchronized to a clock signal of the clock input end to a second node during a period other than a period during which the carry signal is output; and holding units which provide a back-bias voltage to the third output end in response to a signal output from the second node.

[0014] In an exemplary embodiment, the inverter may include at least two transistors connected to a first voltage having a lower voltage level than a low level of the gate signals.

[0015] In an exemplary embodiment, the at least two transistors may be back-biased by one of the back-bias voltage or the compensation signal.

[0016] In an exemplary embodiment, the inverter may include: a first inverter transistor connected to a first voltage having a lower voltage level than a low level of the gate signals; and a second inverter transistor connected to a second voltage having a same voltage level as the low level of the gate signals.

[0017] In an exemplary embodiment, the first inverter transistor may be back-biased by one of the back-bias voltage and the compensation signal.

[0018] In an exemplary embodiment, the stage of the plurality of stages may further include a first pull-down transistor including a control end connected to the third input end to receive the third input signal, a first end connected to the third output end, and a second end connected to the back-bias voltage.

[0019] In an exemplary embodiment, the holding units may include: a first holding transistor including a control end connected to the second node and connected through a third node between the back-bias voltage and the third output end; and a second holding transistor including a control end connected to the second node and connected through the third node between the back-bias voltage and the